REMARKS

Claims 1-26 were examined and reported in the Office Action. Claims 1-26 are rejected. Claims 3, 5-6, 8, 13-14, 16 and 22 are canceled. Claims 1, 2, 4, 7, 9-12, 15, 17, 18, 21, 23 and 24 are amended. Claims 1, 2, 4, 7, 9-12, 15, 17-21 and 23-26 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §102(e)

It is asserted in the Office Action that claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Patent No. 6,374,367 issued to Dean et al ("Dean").

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 1 contains the limitations of

> selecting a phase threshold value, receiving a plurality of branch trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses, determining a plurality of branch address vectors from the plurality of branch addresses, determining histogram bins from the plurality of branch address vectors, determining a distance between centers of at least two consecutive histogram bins, comparing the distance with said selected threshold value, determining major execution phases of an executable process based on the comparison, and using the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Applicant's amended claim 7 contains the limitations of

> select a phase threshold value, receive a plurality of branch trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses, determine a plurality of branch address vectors from the plurality of branch addresses, determine histogram bins from the plurality of branch address vectors, determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, compare the distance with said selected threshold value, determine major execution phases of an executable process based on a result of the compare, and use the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Applicant's amended claim 15 contains the limitations of

> a processor coupled to one of a main memory and a cache memory, at least one process to communicate with said memory, and a phase detector that operates to determine major execution phases of said at least one process to determine where compiler optimization is needed to improve performance of the at least one process in a managed run-time environment.

Applicant's amended claim 21 contains the limitations of

> a first device having a first processor coupled to a first memory and at least one process to communicate with said first memory, and a second device having a second processor coupled to a second memory and at least another process to communicate with said second memory, wherein a phase detector process operating in one of said first processor and said second processor operate to determine major execution phases of one of said one process and said another process within one of said first device and said second device for determining where compiler optimization is needed for one of said one process and said another process to improve performance in a managed run-time environment.

Dean discloses a monitoring system that gathers load and store latencies via a random sampling for *scheduling optimization*. Dean does not teach, disclose or suggest determining where major execution phases exist for *compiler optimization* in *a managed run-time environment*. That is, Dean does not teach, disclose or suggest Applicant's claim 1 limitations of

> determining major execution phases of an executable process based on the comparison, and using the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment,

Applicant's claim 7 limitations of

> determine major execution phases of an executable process based on a result of the compare, and use the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment,

Applicant's claim 15 limitations of

> determine major execution phases of said at least one process to determine where compiler optimization is needed to improve performance of the at least one process in a managed run-time environment,

nor Applicant's claim 21 limitations of

> a phase detector process operating in one of said first processor and said second processor operate to determine major execution phases of one of said one process and said another process within one of said first device and said second device for determining where compiler optimization is needed for one of said one process and said another process to improve performance in a managed run-time environment.

Therefore, since Dean does not disclose, teach or suggest all of Applicant's amended claims 1, 7, 15 and 21 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Dean. Thus, Applicant's amended claims 1, 7, 15 and 21 are not anticipated by Dean. Additionally, the claims that directly or indirectly depend on claims 1, 7, 15 and 21, namely claims 2 and 4, 9-12, 17-20, and 23-26, respectively, are also not anticipated by Dean for the same reason.

Accordingly, withdrawal of the 35 U.S.C. §102(e) rejections for claims 1-26 are respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1, 2, 4, 7, 9-12, 15, 17-21 and 23-26, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Jean Svoboda Date: April 23, 2007